Integrating Electronics Update

This is supposed to be a quick summary of items and ideas discussed during the November 15, 16 meeting, some of which I believe require input from the collaboration:

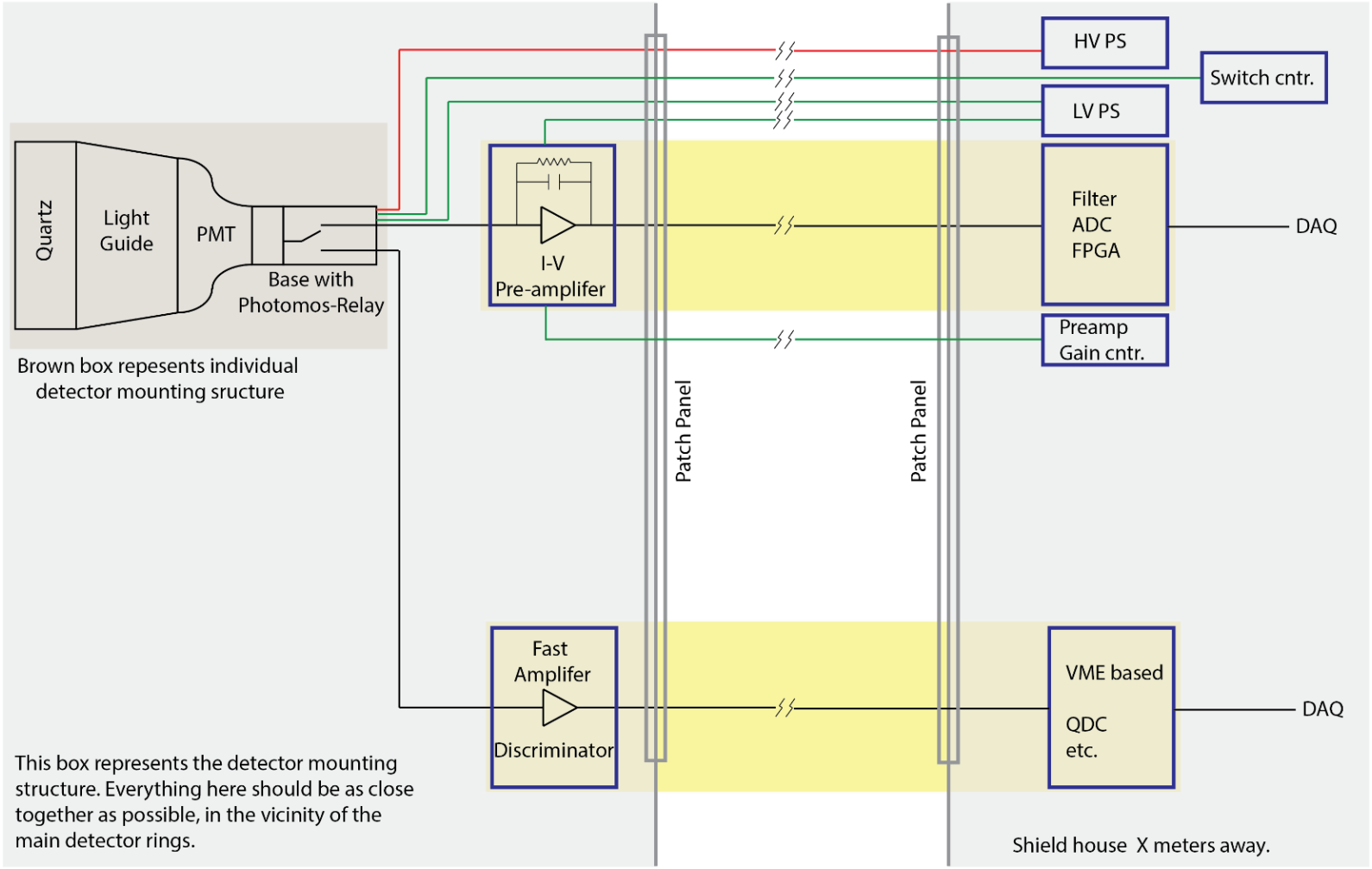
- **Preamp interface with PMT base**
  - Directly attach preamp to PMT base with suitable connector (no cable)
  - Preamp gets ground from PMT HV
  - Separate ground isolated power supply for preamp and base switching
- **Preamp design changes – power supply and differential driver**
  - No DC-DC converter (problem – higher bandwidth mixes switching noise into the signal band)
  - Use ground isolated power supply and a voltage regulator instead
  - Use fully differential signal from the preamp to the ADC board
- **Cabling between preamp and ADC board – fully differential signal**
  - Shielded twinax cable from preamp to ADC
- **ADC board design**
  - See next couple of slides …

Present at the meetings:

Sebastian Baunack, Igor Beltschikow, Jürgen Diefenbach, Michael Gericke, Rahima Krini, Werner Lauth, Frank Maas

Integrating Electronics

Reminder:



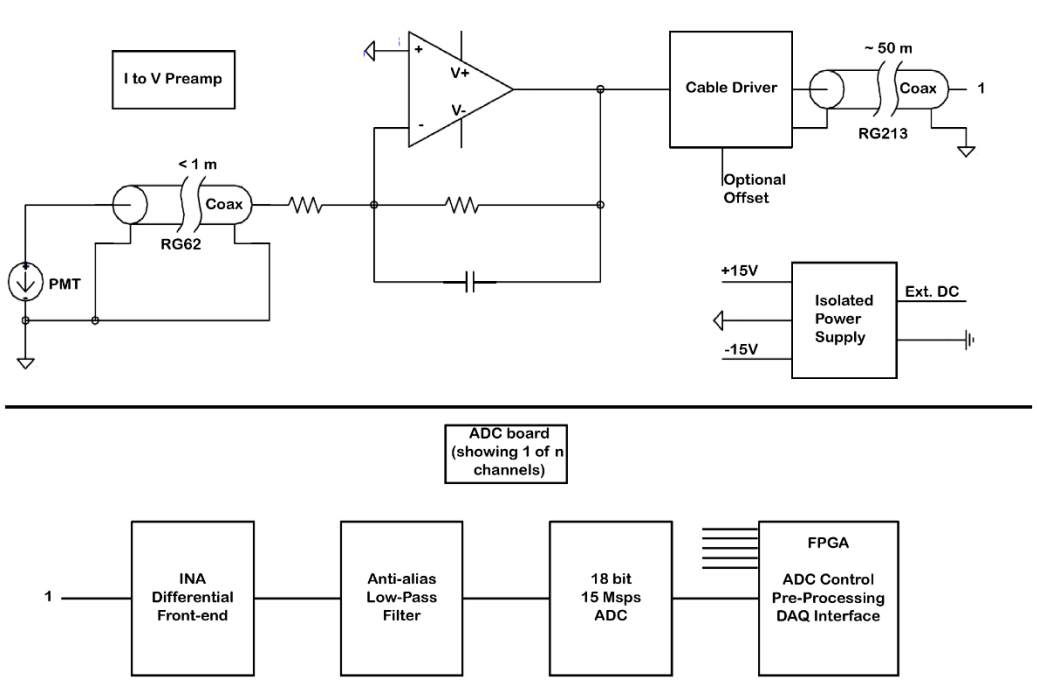
Main Front-end Components

Reminder:

1. PMT
2. I-V Pre-amplifier
3. Filter stages
4. ADC
5. FPGA

Main parameters (some assumptions):

- PMT gain: $\gtrsim 1000$
- Avg. cathode current: $\sim 10\ pA$
- Preamp gain: $10's \rightarrow 100's\ k\Omega$
- Bandwidth: $\sim 1\ Mhz$
- Sampling rate: $15\ Msps$
- Ampl. resolution: $18\ bit$

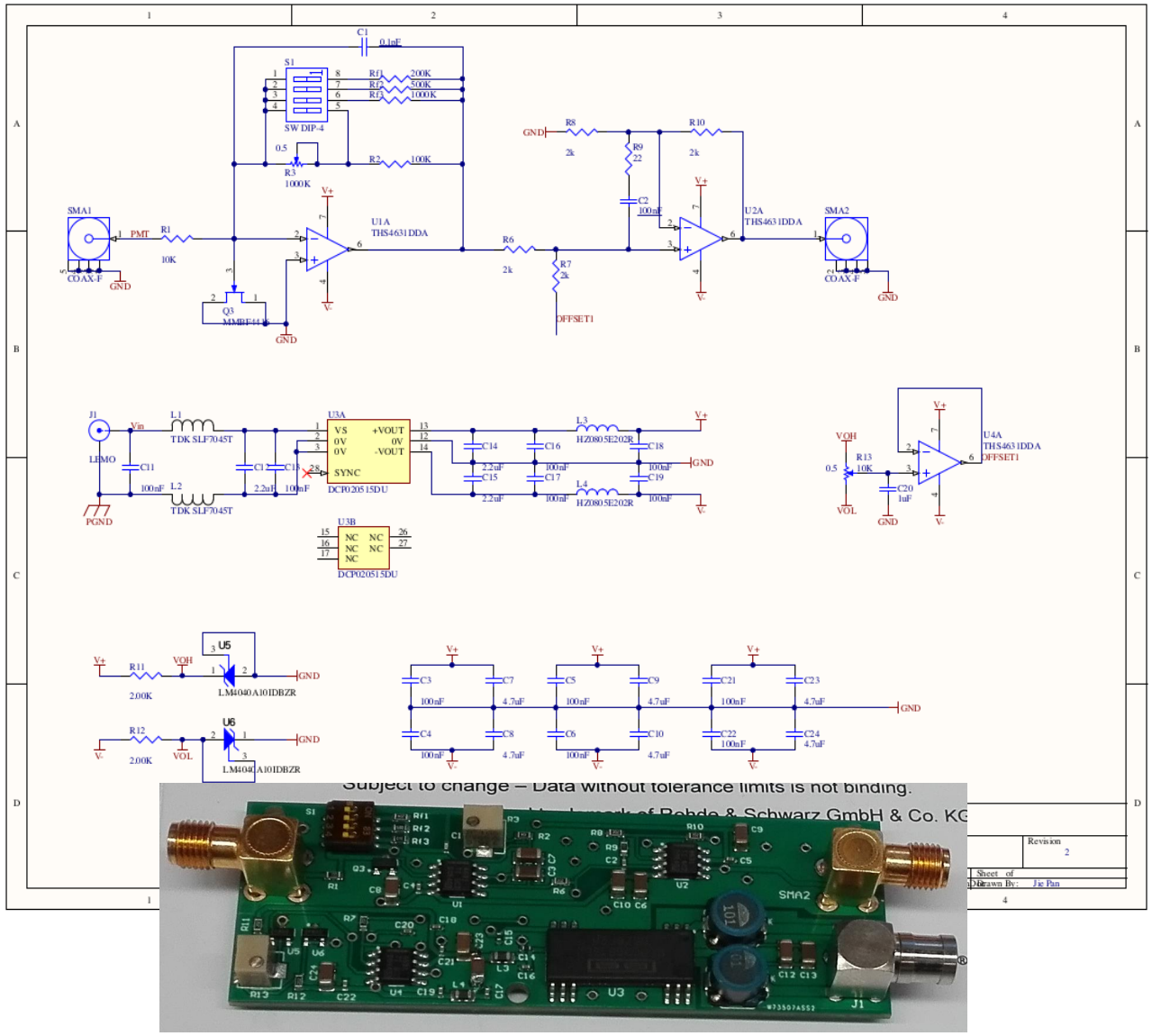


FPGA

- Sums 15 Msps down to helicity window data items
- Buffers the data
- Serializes and controls data transfer
- Takes external clock and gate

New design of the preamp

First preamp prototype:



Inherited Qweak design:

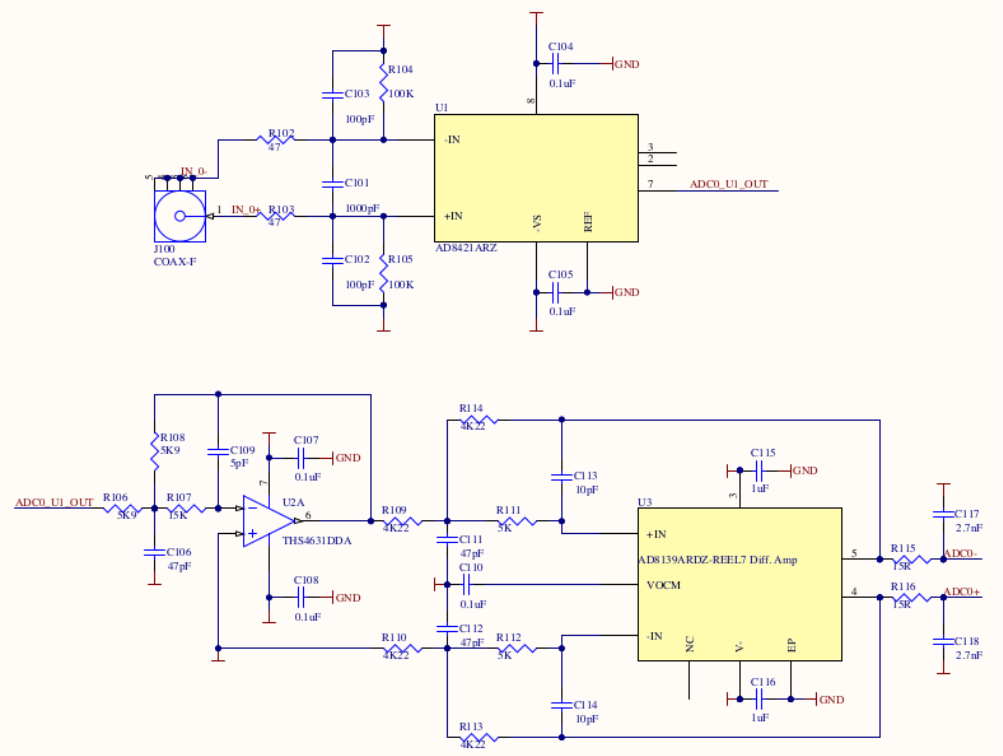
- Two stages in the circuit: I-to-V & cable driver
- Selectable trans-impedance gain (0.1 – 1.0 MΩ in this design)
- Isolated DC-DC converter 5 V external -> ±15 V internal
- Replaced Qweak OPAmps (OPA2604) with THS4631 to reach the bandwidth requirement for Moller:

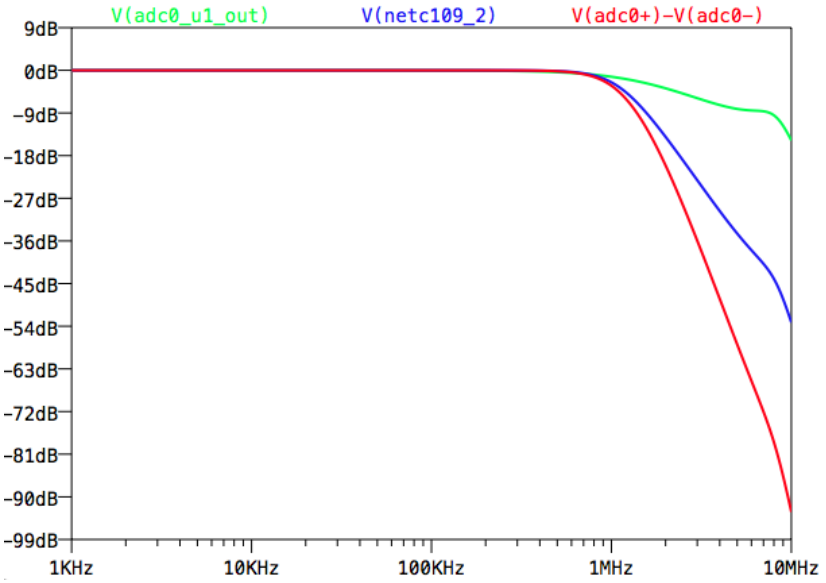
DC-DC converter has 800 kHz switching noise, which is in our new bandwidth …

Updates / Progress (slides from Jie)

ADC Board

Anti-alias filter design (schematics & spice simulation)



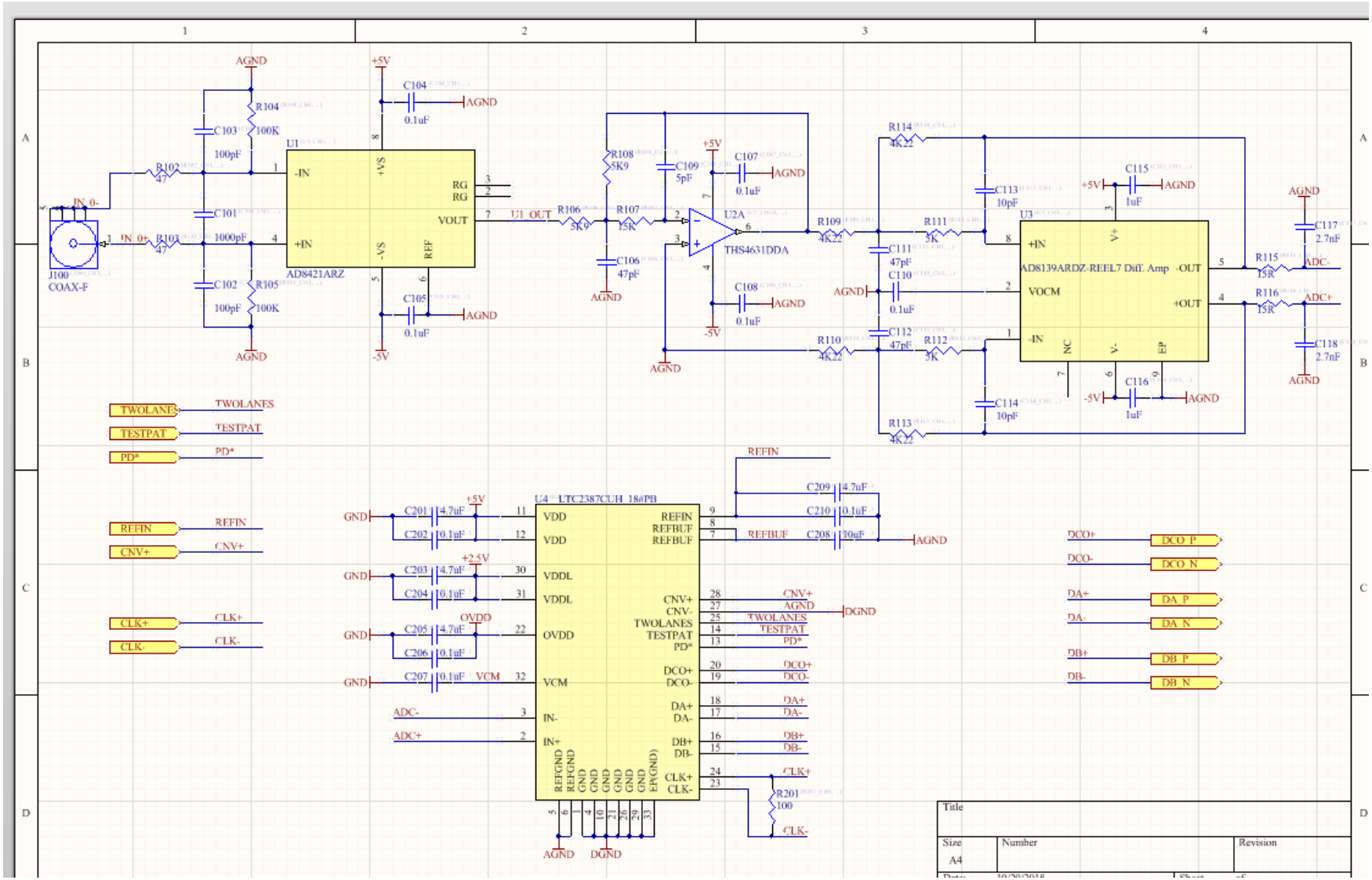


- *Sharp cut-off frequency appears ~1 MHz;*
- *Flat top gain response goes up to ~800 kHz.*

Simulated results:

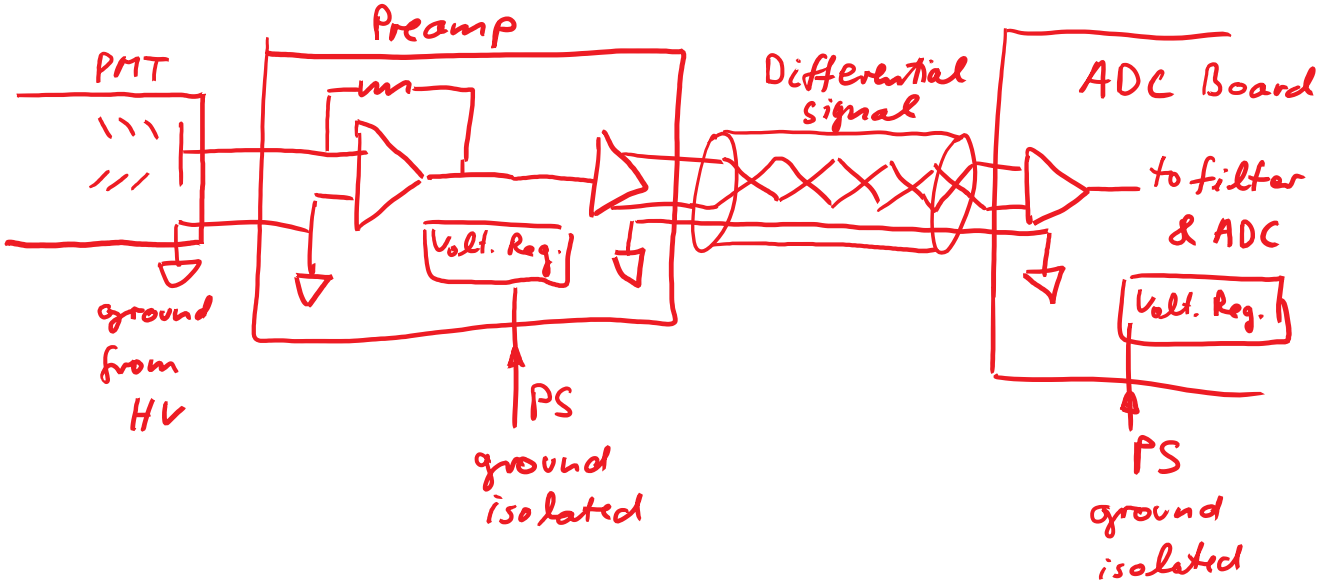
Solid lines – relative gains
Green, blue and red lines – output signals of first (AD8421), second (THS4631) and third (AD8139) IC

ADC Board Front-End Design

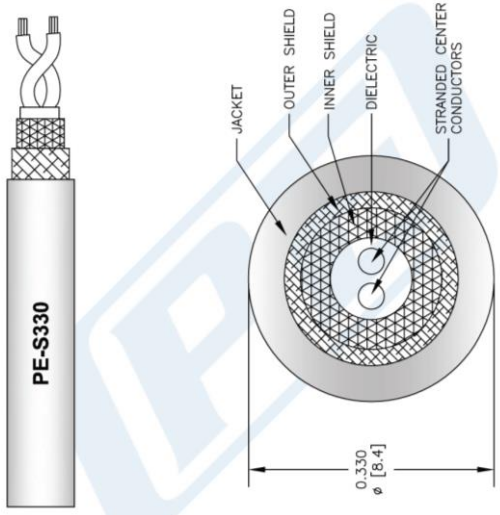


New design of the preamp

Suggestion for new grounding scheme (sorry no nice schematic yet):



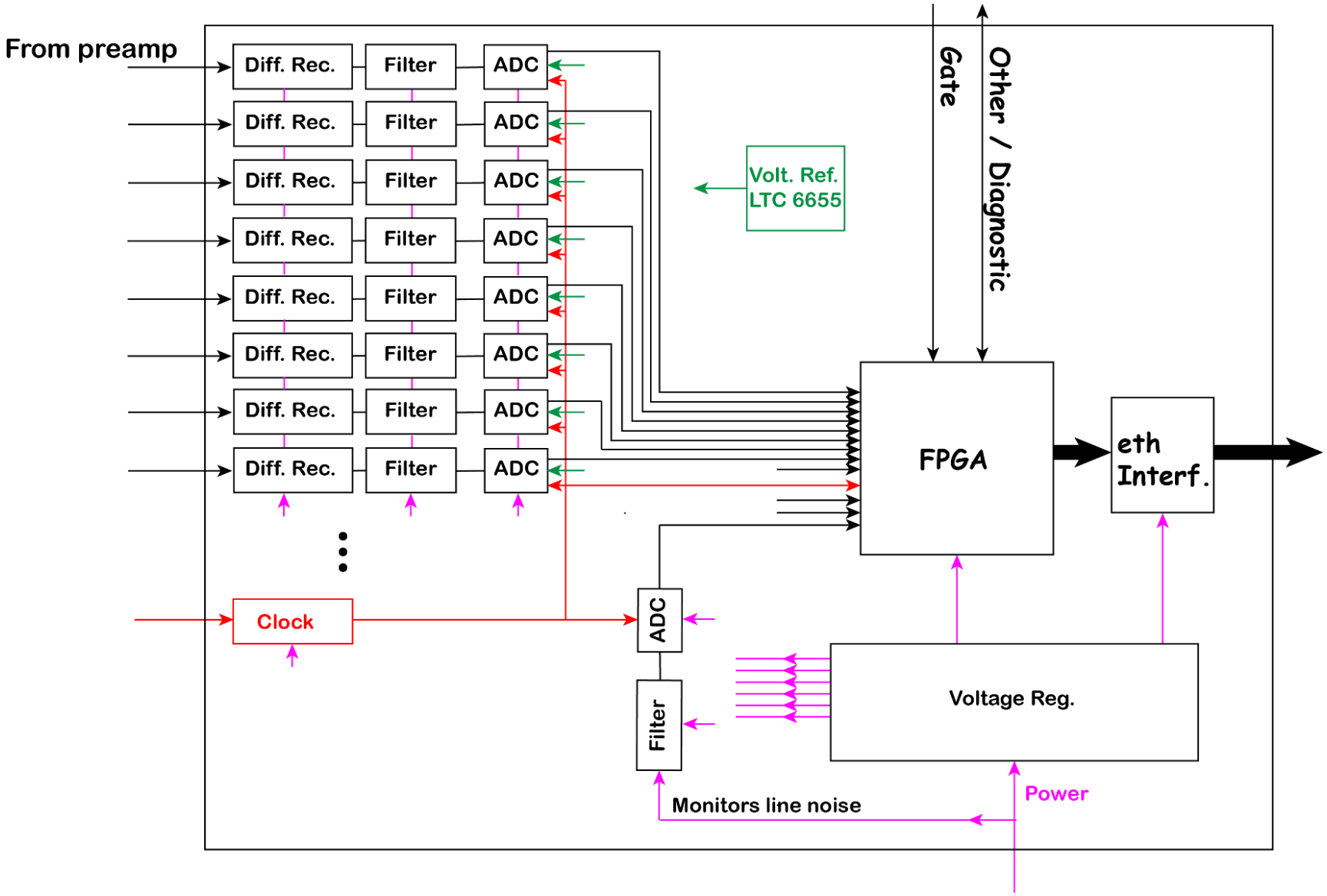
- Ground comes from PMT HV only
- Everything else is connected to ground isolated power supplies
- Use voltage regulators on each board, each with its own PS channel
- Use a well designed differential transmitter and receiver pair between preamp and ADC board
- ADC board grounded through preamp (unclear how this works with several preamp channels per board – ground loops ?)
- Suggested cable: Shielded Twinax



Notes on ADC board design

- Want to switch between high rate streaming (read out all samples) and FPGA preprocessing based in helicity window information
- Switching must be done via TTL input (not FPGA reprogramming) and should have ability to digitally select channels to read out in high rate mode
- ADC sampling rate must be the same in both modes
- Provide separate ADC channel that digitizes PS line noise on each board
- Use external clock for synchronization and separate on-board PLL to provide clock signal to all components (ADC, FPGA, etc.) – meaning do not use FPGA to distribute clock signals (too much jitter)
- External (GPS) clock up to 125 MHz
- Explore moving to 10 Gbit ethernet transfer off the board and use TCIP protocol (lossless)

ADC Board Block Diagram



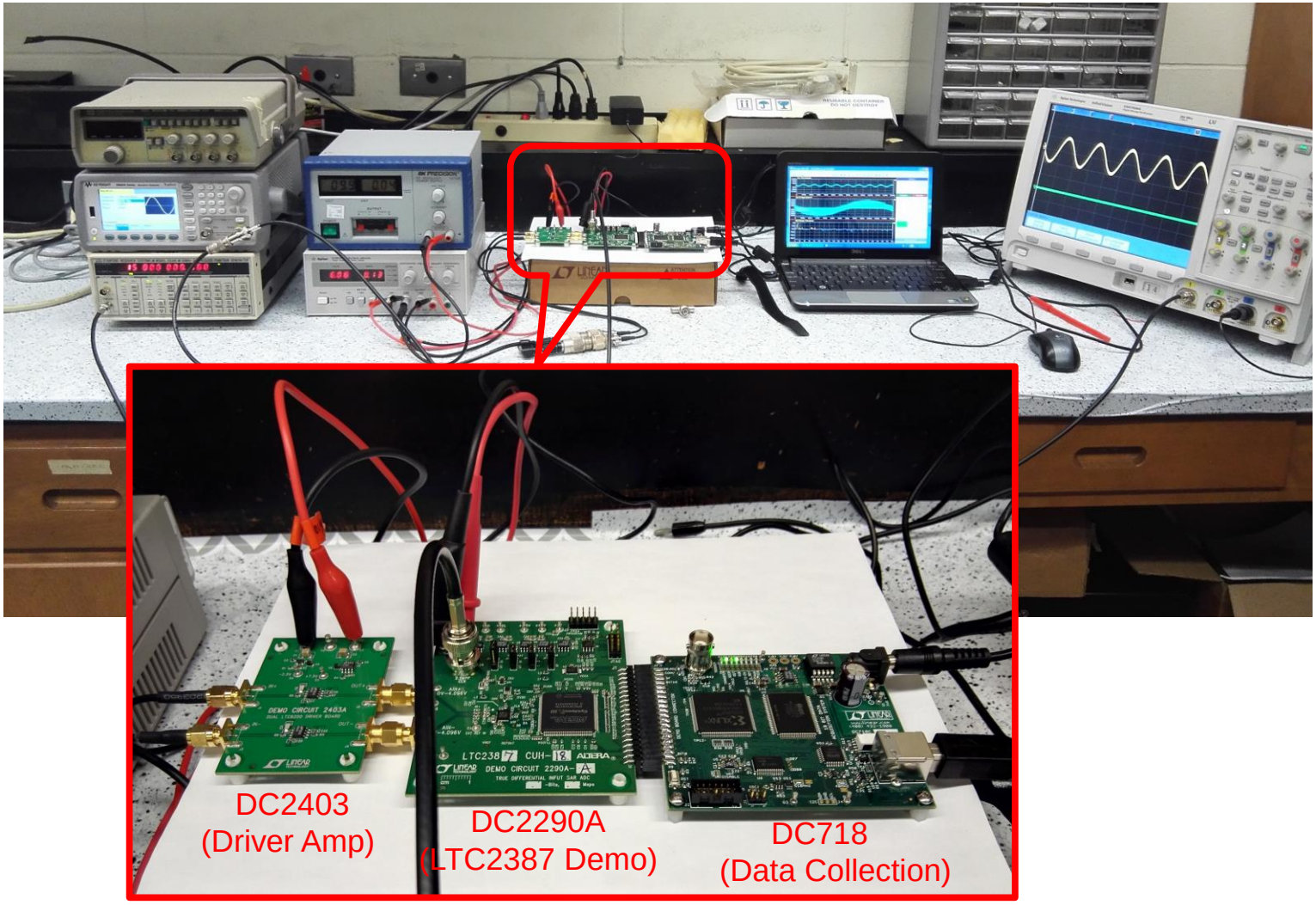
Backup Slides

Updates / Progress (slides from Jie)

ADC Board

ADC (candidate - LTC2387 18-bit ADC)

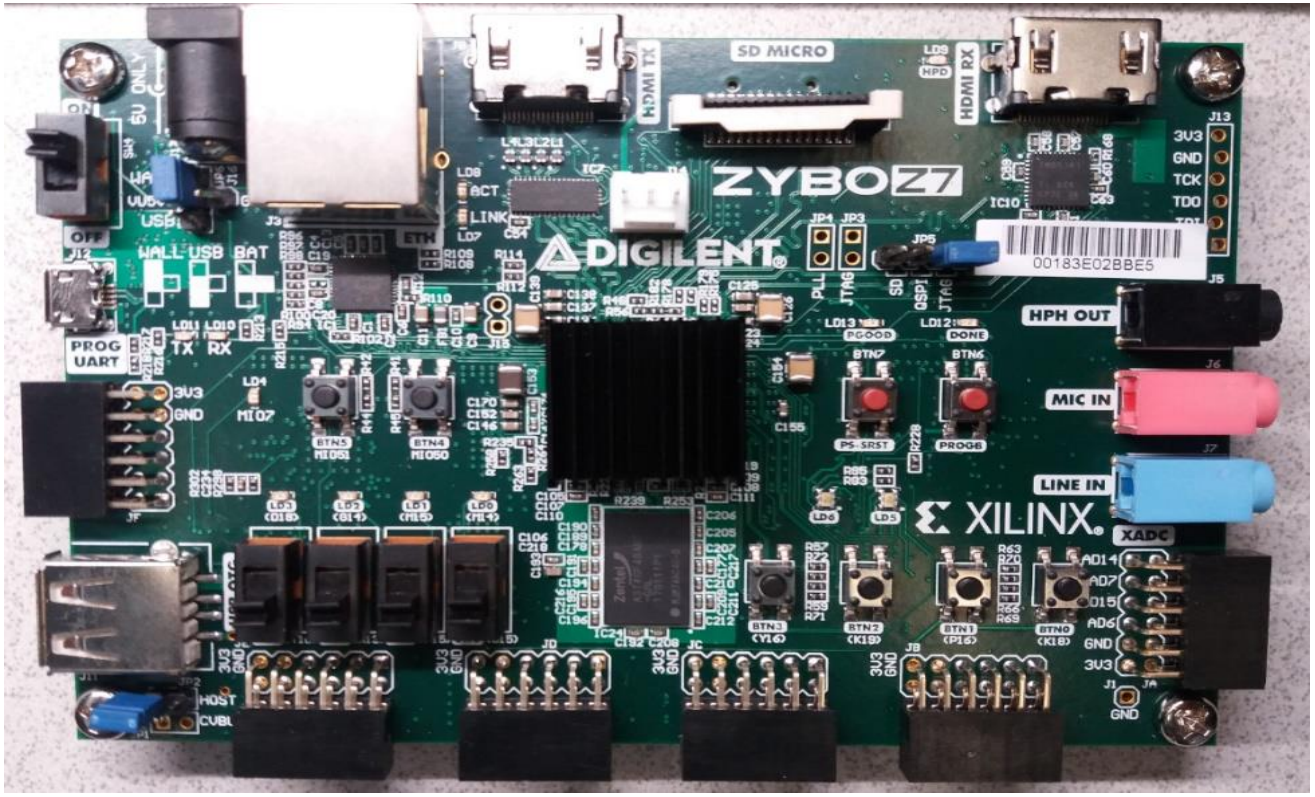
Bench Test Setup with LTC2387-18 evaluation board:



Updates / Progress

ADC Board

FPGA (candidate – Zynq-XC7Z020-1CLG400C)



The FPGA evaluation board is under test; a very preliminary test firmware has been implemented.

Data Bandwidth and Transfer

- Use continuous sampling of filtered preamp signal with gated collection of data
  - Currently considering a 15 Msps, 18 bit ADC
  - At production helicity rate: Read out data for each helicity window separated into 4 blocks and all together = 5 data units
    - Each data unit consists of 4 items: The mean, minimum, maximum, and rms of the collected samples (calculating these is done in the FPGA)
    - At 15 Msps ~6900 ADC samples per block from which to calculate these
    - 4 bytes for each data item in 5 data units = 80 bytes / channel / window
    - 8 bytes for one timestamp per helicity window -> 88 bytes / channel /window
    - 8 channels per board with one readout link -> $<$ 1kB / helicity window per board
  - For diagnostic purposes readout every ADC sample
    - Data link and protocol determine the maximum "event" rate …

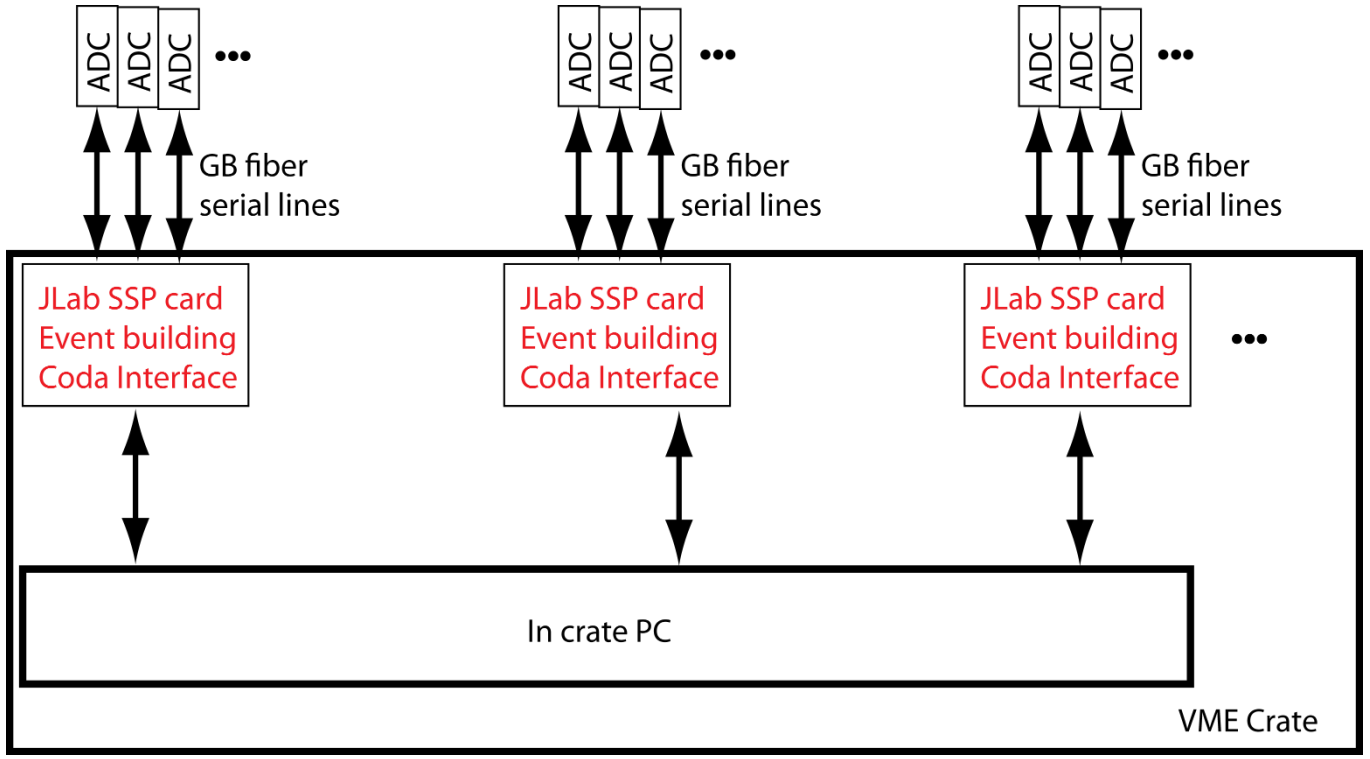
Data Bandwidth and Transfer

- Gigabit Ethernet: ~600 Mbit/s
  - Means roughly 37 kbytes/helicity window at production (1.92 kHz) reversal (we have a lot of head room with this)
  - But can the FPGA handle this …
  - What protocol is suitable for CODA ?
    - e.g. UDP ?
    - 8bit/10bit standard IBM encoding ?
    - TCPIP
    - Other ?

Data Bandwidth and Transfer

- Meeting between Paul King, Dave Abbott, and Bob Michaels to discuss interface options to JLab system:

Synchronization taken care off by SSP module and TS

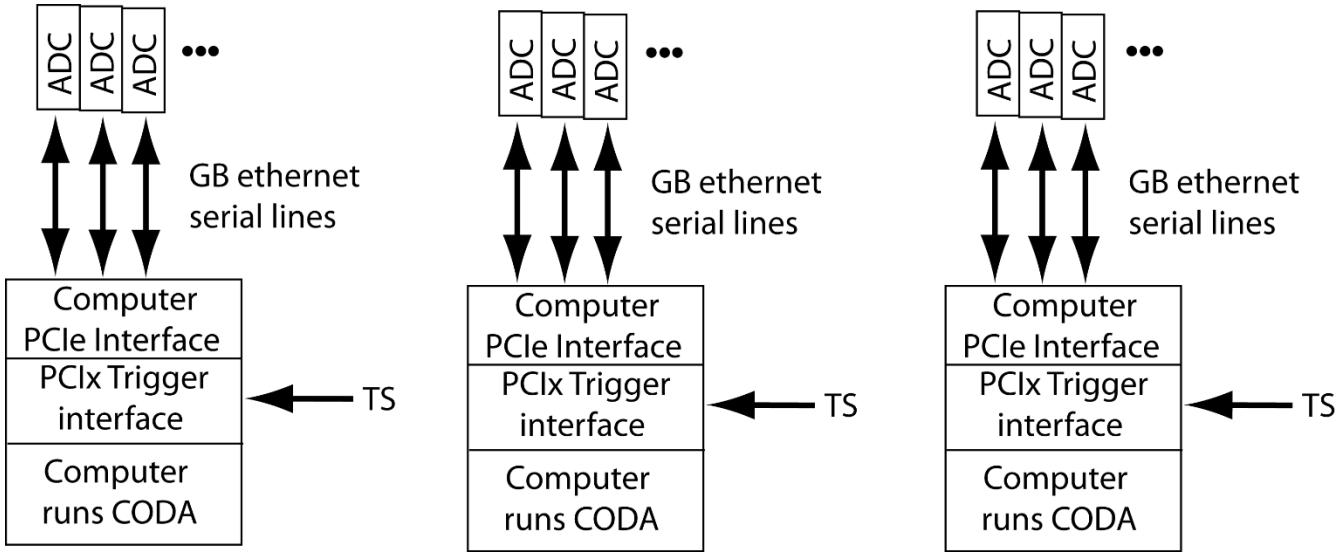


Computers need to be synchronized by a common clock

Data Bandwidth and Transfer

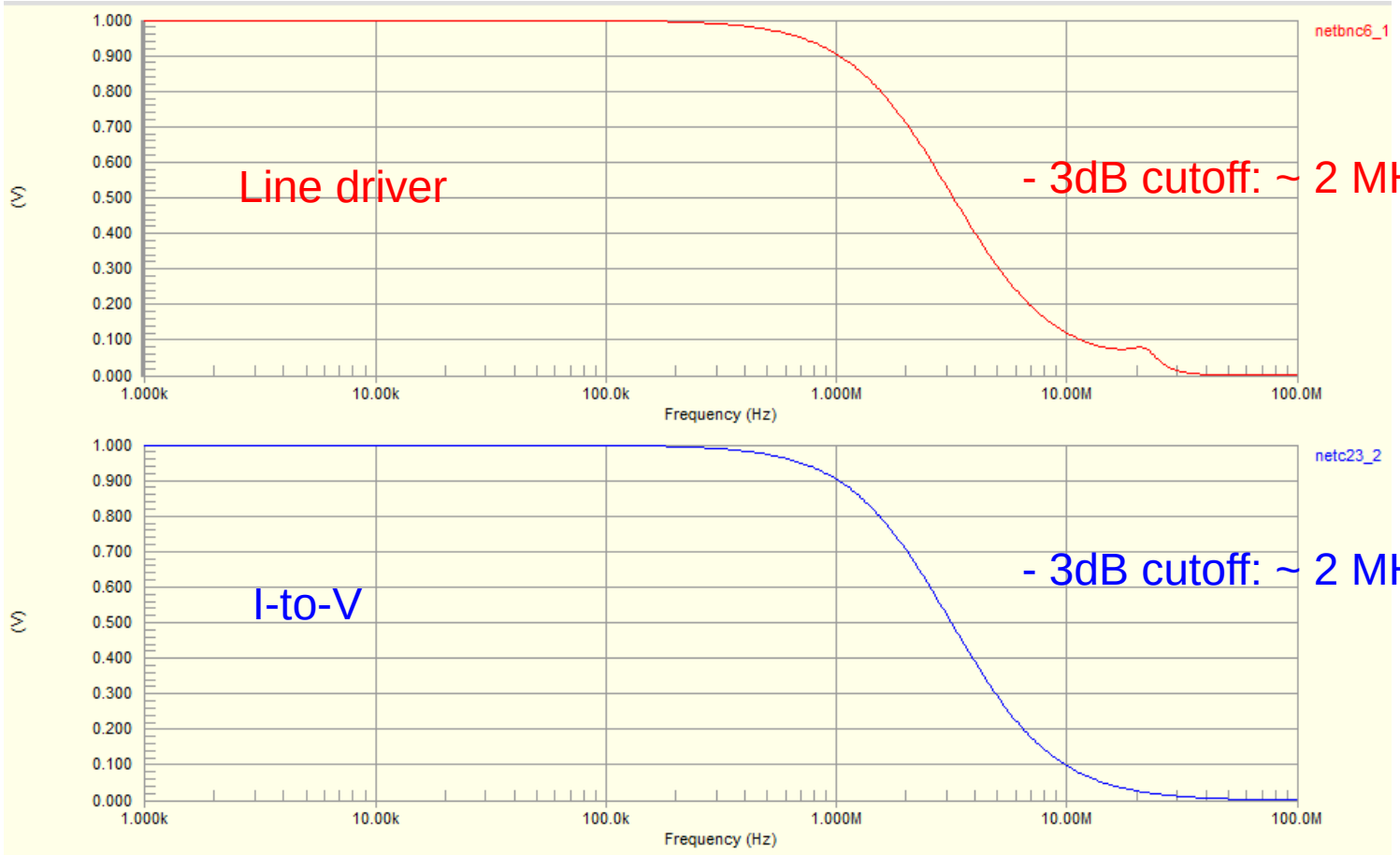
- Meeting between Paul King, Dave Abbott, and Bob Michaels to discuss interface options to JLab system:

Computers need to be synchronized by a common clock



Updates / Progress (slides from Jie)

Spice simulation



Frequency response at gain = 1 MΩ, with 1 V sine wave input
(assuming input and load capacitance = 0)

Updates / Progress (slides from Jie)

Preamp prototype (5 made for testing):

Molex RF connector (input signal)

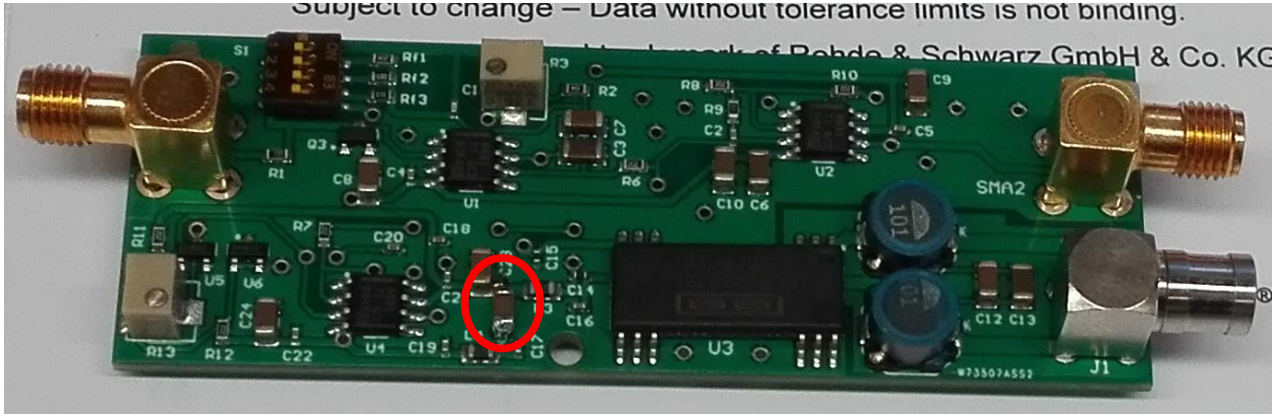
DIP switch for gain adjustment

Molex RF connector (output signal)

SMB connector (power supply)

Updates / Progress (slides from Jie)

Preamp prototype (5 made for testing):



- This preAmp board consumes more power than the Qweak preAmp:

  Our Prototype PreAmp – 5 V / 250 mA; (THS4631 consumes more power)
  Qweak PreAmp – 5 V / 150 mA.

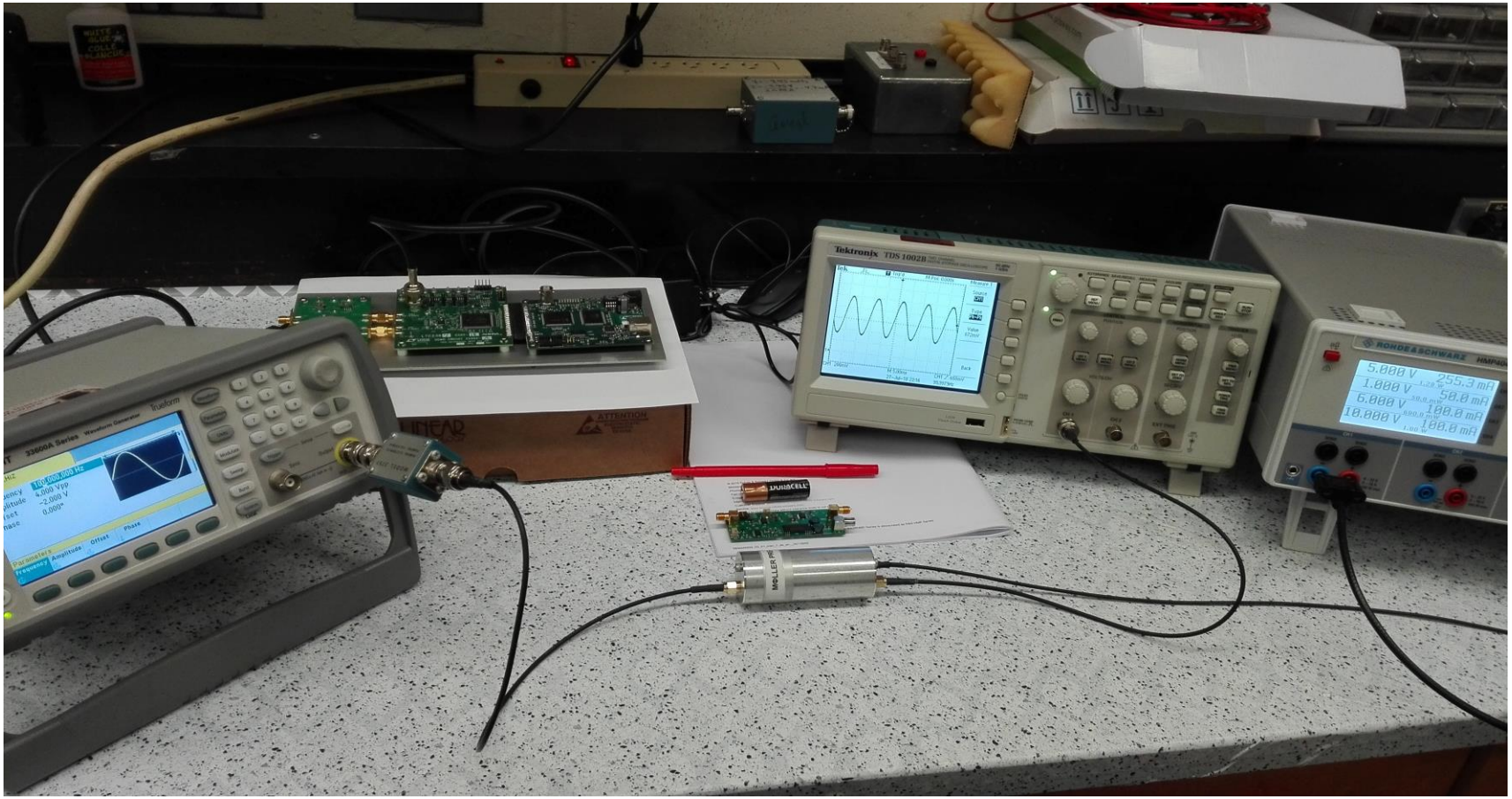
  Larger ripples arise due to higher current

- Smaller PCB size (8 cm x 3 cm) leads to larger interference from the PS switching noise.

- Based on our tests, the size of the ripples could be significantly reduced by using larger capacitor in the isolated PS circuit – probably have to change the PS

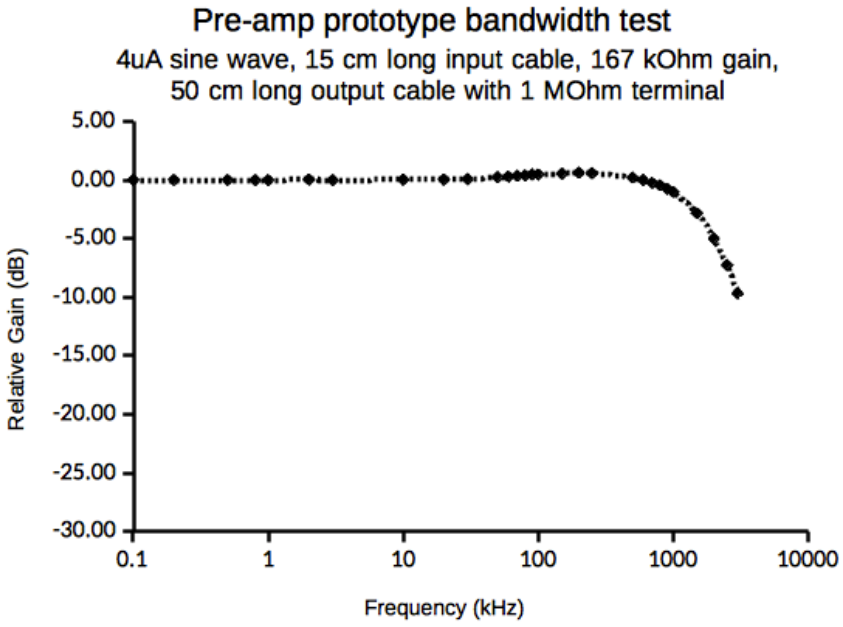
Updates / Progress (slides from Jie)

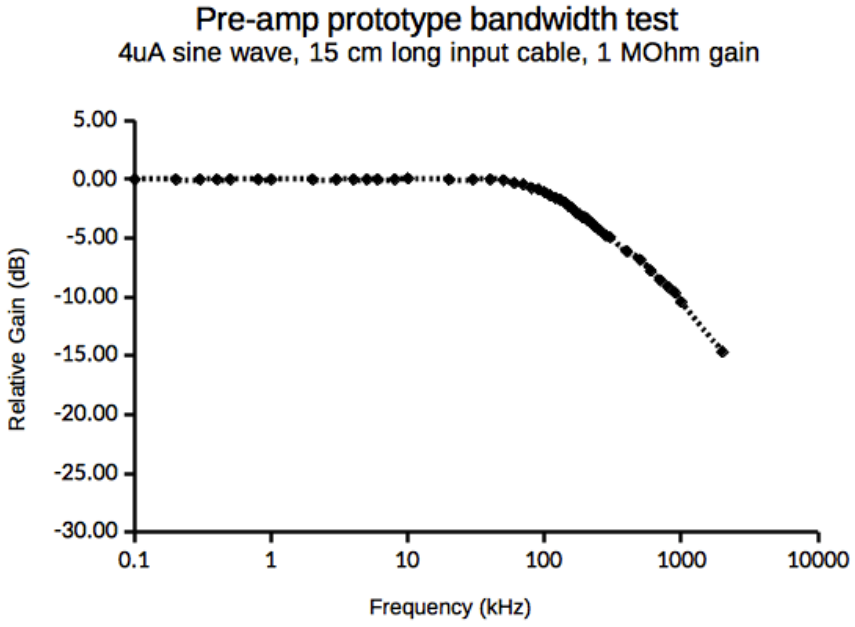
Prototype tests



Updates / Progress (slides from Jie)

Testing the effects of the transimpedance gain on bandwidth





* Bandwidth Tests with Sine-wave input (4 uA p-p, -2 uA offset)

The smaller transimpedance → ***larger bandwidth***

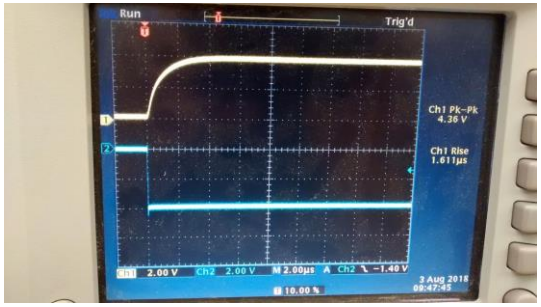
Probably need a two-stage amplifier (next prototype)

Updates / Progress (slides from Jie)

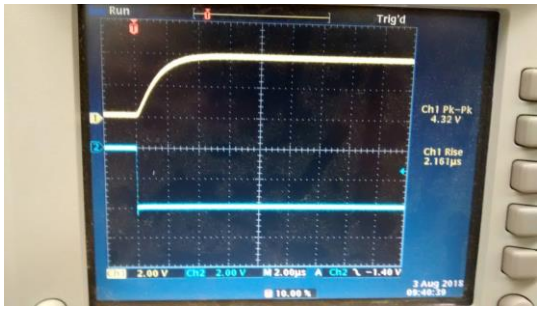
Prototype tests under various run conditions

Testing the pulse response of the preAmp to the input cable length

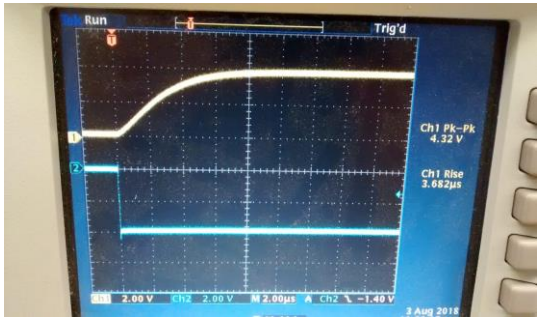
Ch2 (Blue): Input -4 μA current pulse, Ch1 (yellow): preamp output



Input cable length: **15 cm**
Input cable capacitance: 15pF
Rise time: 1.6 μS
Settling time: 3 μS



Input cable length: **55 cm**
Input cable capacitance: 55pF
Rise time: 2 μS
Settling time: 4 μS



Input cable length: **240 cm**
Input cable capacitance:
240pF
Rise time: 4 μS
Settling time: 8 μS

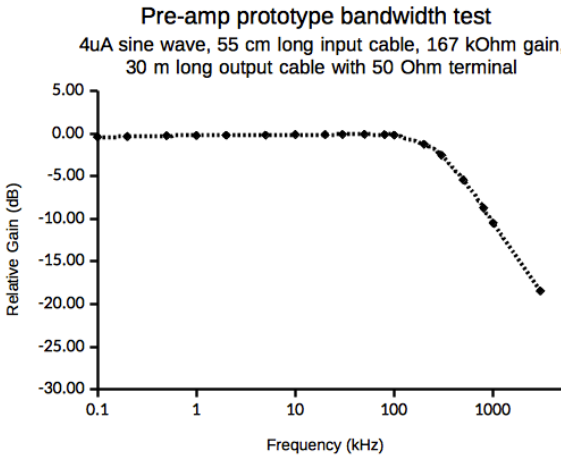
The input cable length must be short enough so that the frontend settling time is less than the helicity reversal settling time.

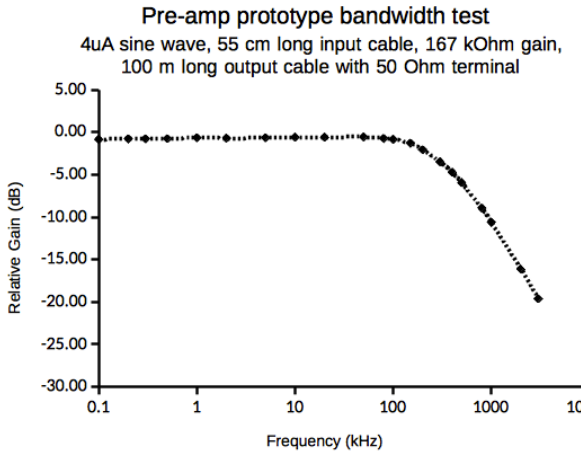
Updates / Progress (slides from Jie)

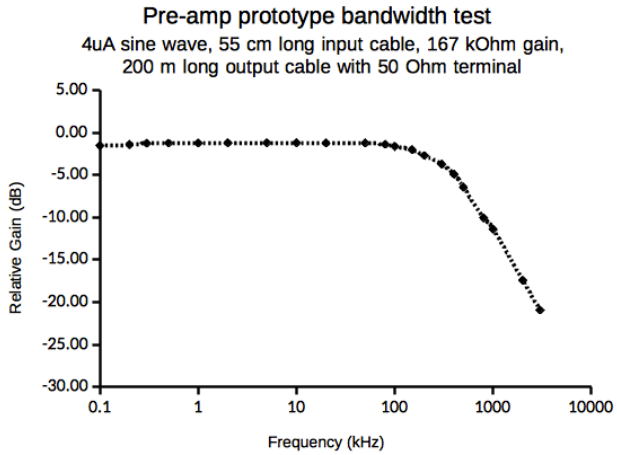
Preamp Prototype tests under various conditions

Testing the capability of the cable driver

Trans-impedance Gain	Length of the input cable	Length of the output cable & terminal	f Cutoff 3dB
167 kΩ	55 cm	30 m & 50 Ω	330 kHz
	55 cm	100 m & 50 Ω	270 kHz
	55 cm	200 m & 50 Ω	230 kHz





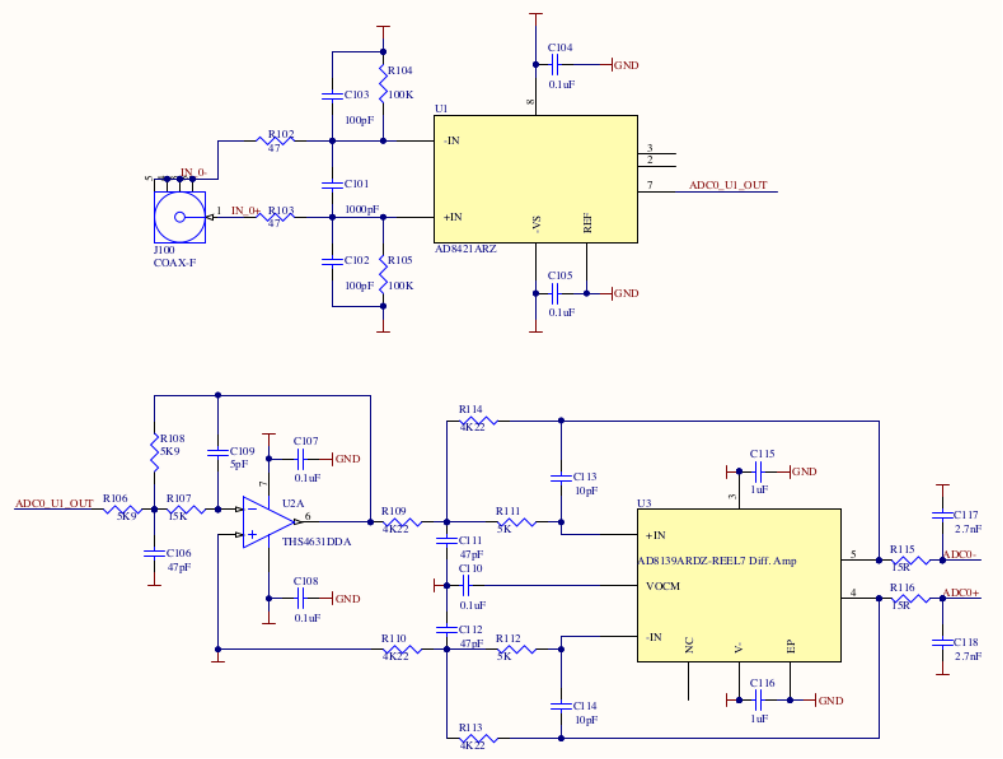


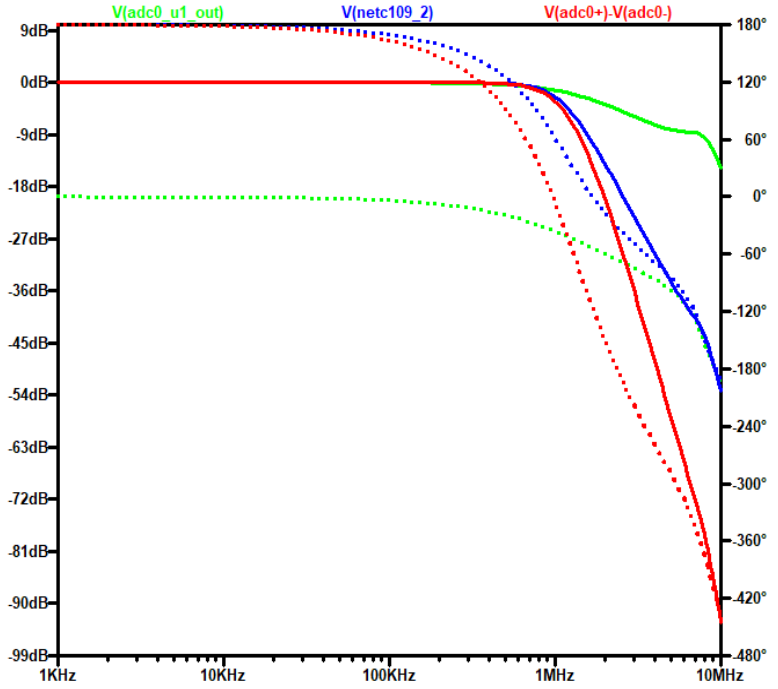
As increasing the output cable length to 200 m, we can see some effects on bandwidth and the relative gain, but the variation on the gain is still small and acceptable.

Updates / Progress (slides from Jie)

ADC Board

Anti-alias filter design (schematics & spice simulation)





Simulated results:

- *Sharp cutoff frequency appears ~1 MHz;*
- *Flat top gain response goes up to ~800 kHz.*

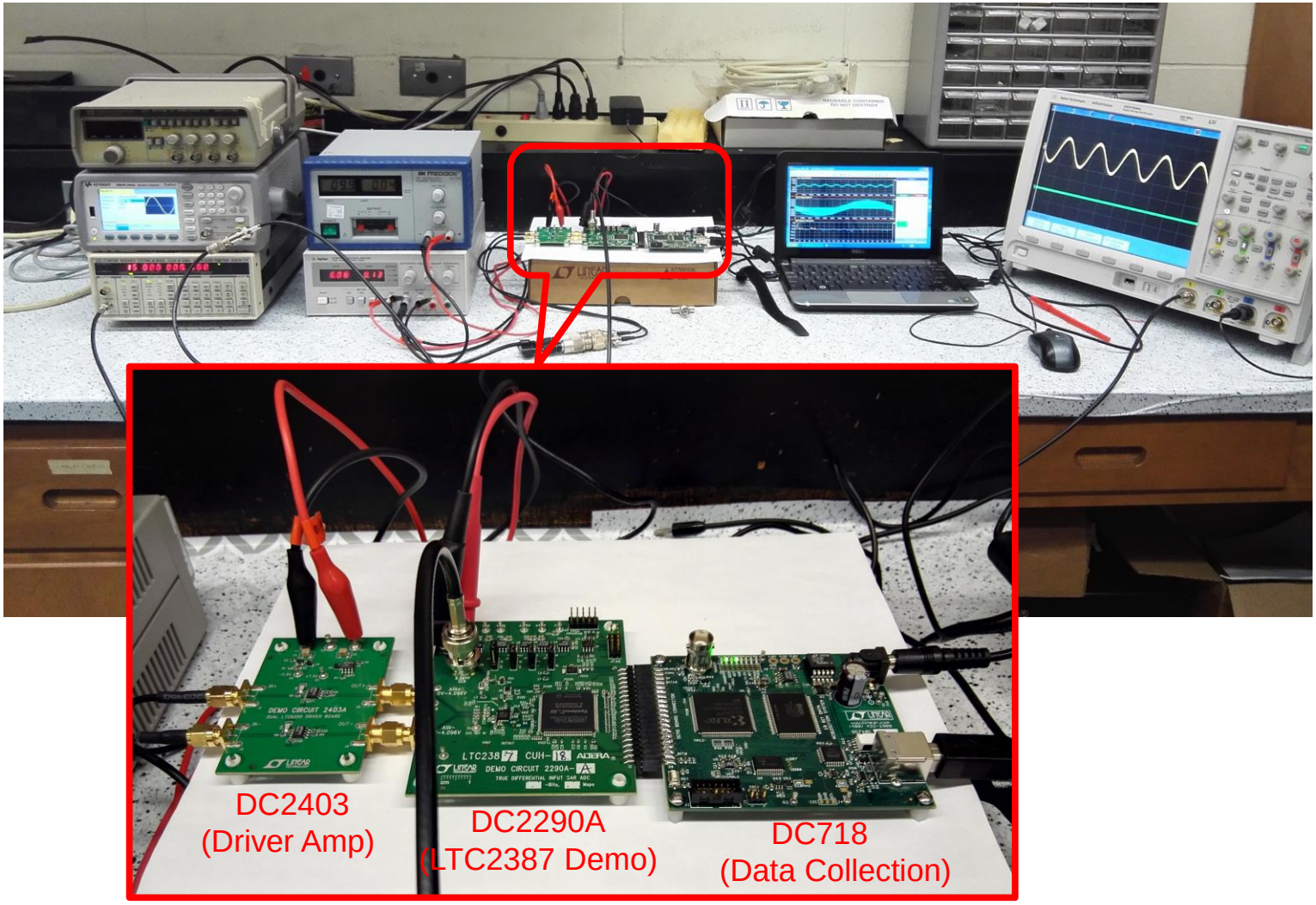
Solid lines – relative gains
Dashed lines – phase shifts
Green, blue and red lines – output signals of first (AD8421), second (THS4631) and third (AD8139) IC

Updates / Progress (slides from Jie)

ADC Board

ADC (candidate - LTC2387 18-bit ADC)

Bench Test Setup with LTC2387-18 evaluation board:

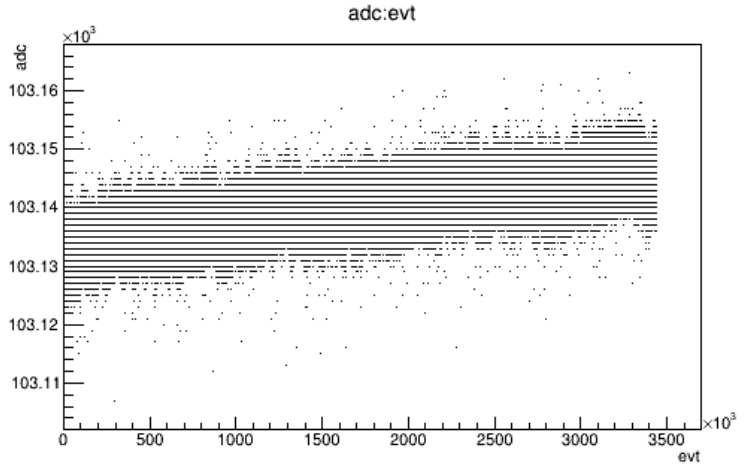


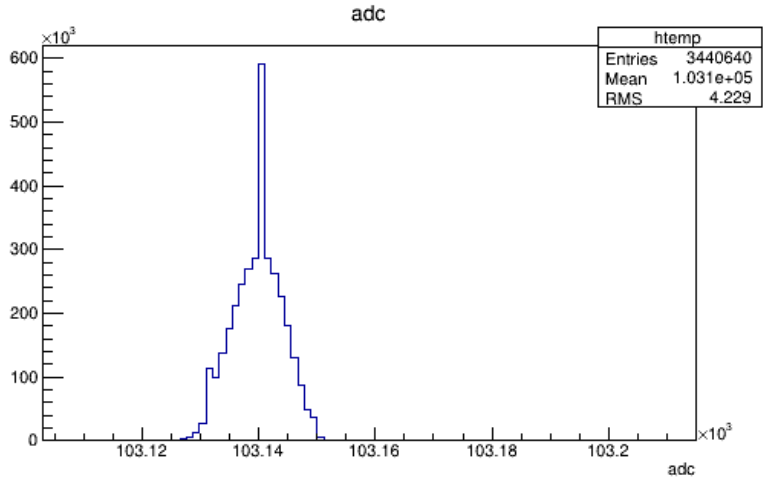
Updates / Progress (slides from Jie)

ADC Board

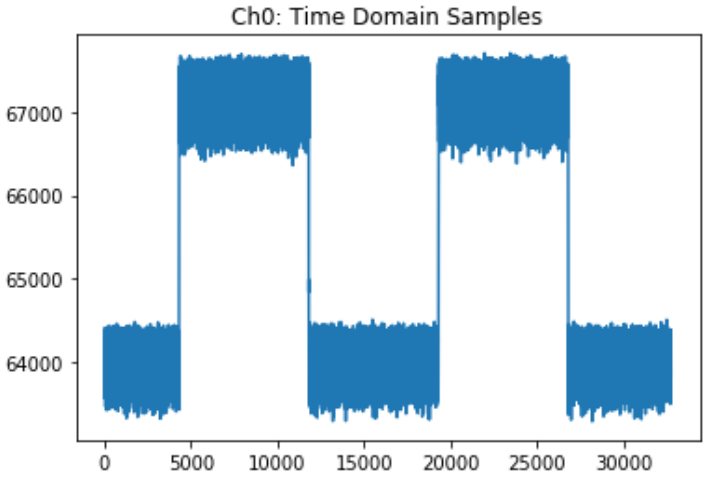
ADC (candidate - LTC2387 18-bit ADC)

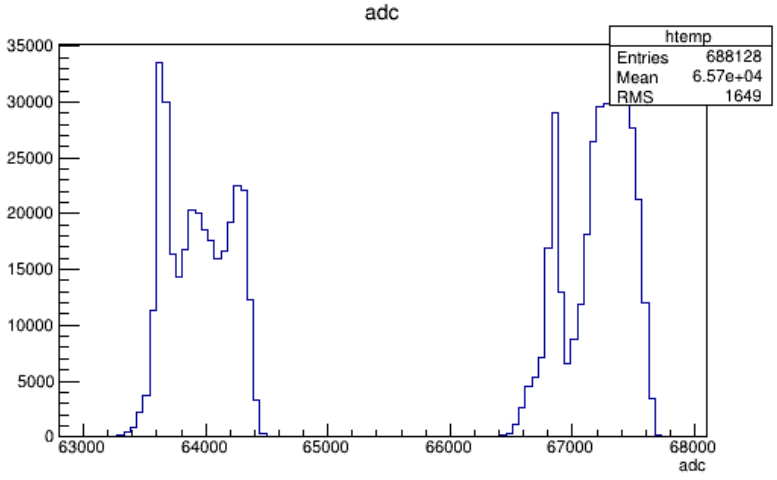
Example 1: RMS noise test with battery (constant voltage source: 3.0 V DC)





Example 2: Square-wave test (input 100 mVpp, V_offset = 2.048 V)

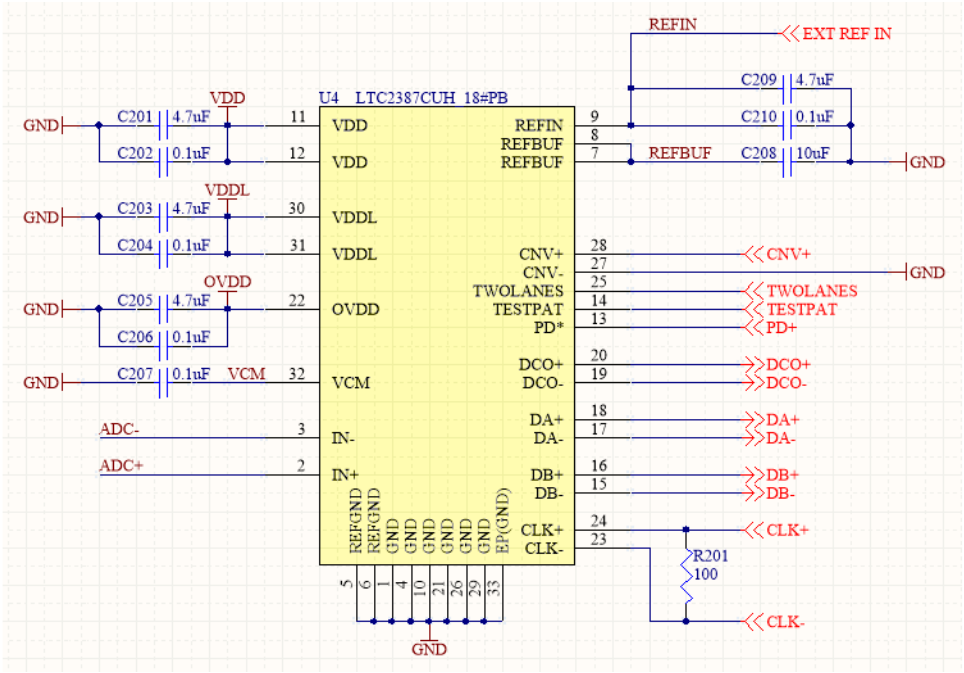


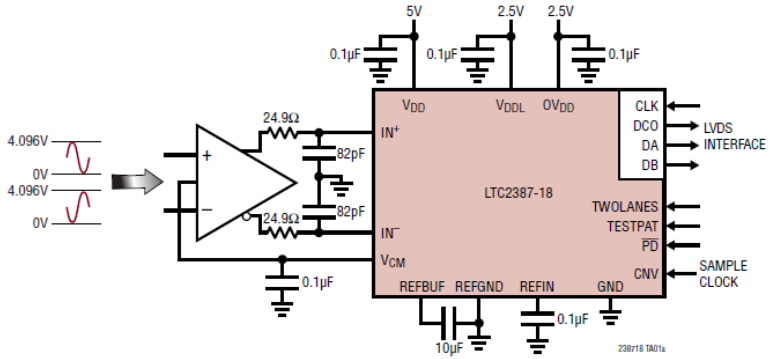


Updates / Progress (slides from Jie)

ADC Board

ADC implemented in the integrator circuit design





(one ADC channel)

The integrator circuit design using LTC2387-18 is underway.
We're planning to implement 16 ADC channels in one PCB board.

Updates / Progress

LINEAR TECHNOLOGY

LTC2387-18

18-Bit, 15Msps SAR ADC

FEATURES

- **15Msps Throughput Rate**
- **No Pipeline Delay, No Cycle Latency**
- **95.7dB SNR (Typ) at f_{IN} = 1MHz**
- **102dB SFDR (Typ) at f_{IN} = 1MHz**
- **Nyquist Sampling Up to 7.5MHz Input**
- Guaranteed 18-Bit, No Missing Codes
- ±3LSB INL (Max)
- 8.192V_{P-P} Differential Inputs
- 5V and 2.5V Supplies
- Internal 20ppm/°C (Max) Reference
- Serial LVDS Interface
- 125mW Power Dissipation
- 32-Pin (5mm × 5mm) QFN Package

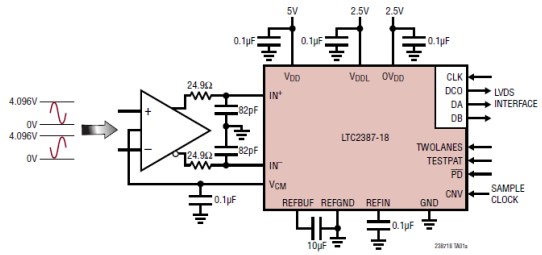
APPLICATIONS

- High Speed Data Acquisition
- Imaging
- Communications
- Control Loops
- Instrumentation
- ATE

DESCRIPTION

The LTC®2387-18 is a low noise, high speed, 18-bit 15Msps successive approximation register (SAR) ADC ideally suited for a wide range of applications. The combination of excellent linearity and wide dynamic range makes the LTC2387-18 ideal for high speed imaging and instrumentation applications. No latency operation provides a unique solution for high speed control loop applications. The very low distortion at high input frequencies enables communications applications requiring wide dynamic range and significant signal bandwidth.

To support high speed operation while minimizing the number of data lines, the LTC2387-18 features a serial LVDS digital interface. The LVDS interface has one-lane and two-lane output modes, allowing the user to optimize the interface data rate for each application.

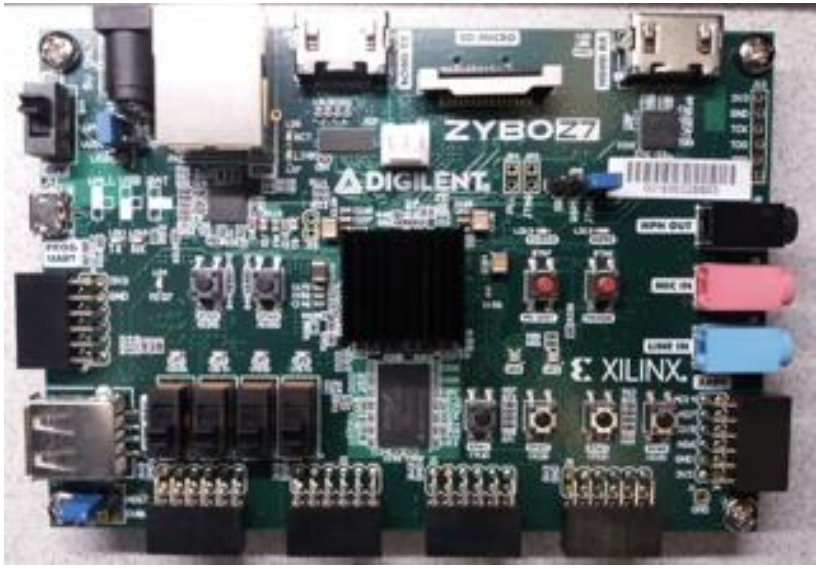


Updates / Progress

ADC Board

FPGA (candidate – Zynq-XC7Z020-1CLG400C)

(for pre-formatting and streaming)



- XC7Z020-1CLG400C is a complete System on Chip (SoC)

Dual core ARM Cortex-A9 processor system (PS), integrated with 28 nm programmable logic (PL);

The PS includes on chip memory 256 kB RAM, external memory interface and tri speed Ethernet MAC peripherial with IEEE std. 802.3; The PL has 140 block of BRAM, 36 kb for each.

- Meet our requirements on speed & memory (/buffering and data transfer)

- 125 pin for general input/output, can interface with 16 ADC channels.

The FPGA evaluation board is under test; a very preliminary test firmware has been implemented.

Electronics Summary/Open Issues

Summary

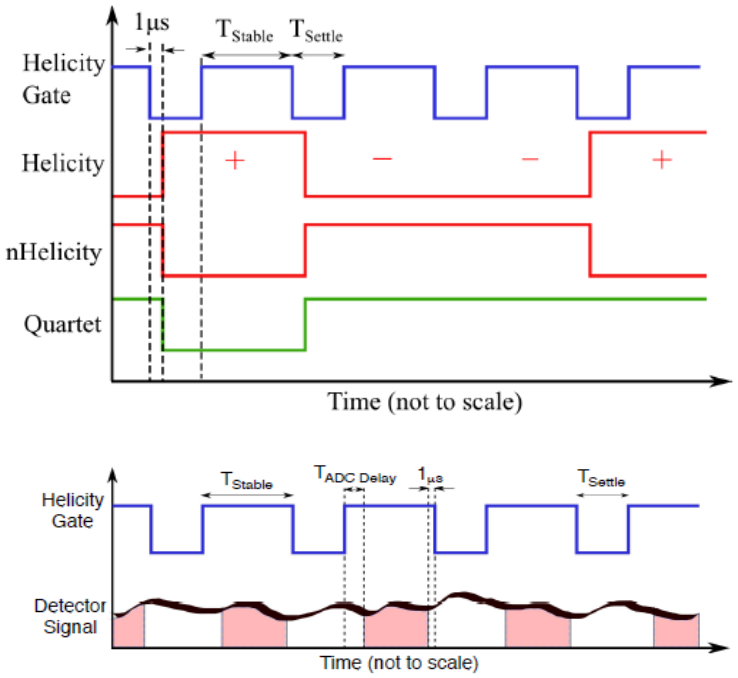
- We are starting to design a prototype PMT base
- We have a first preamp prototype and are bench-testing
- We are testing both the candidate ADC and the FPGA with evaluation boards
- We have started to design the front-end of the ADC board
- We have started to write test firmware for the FPGA

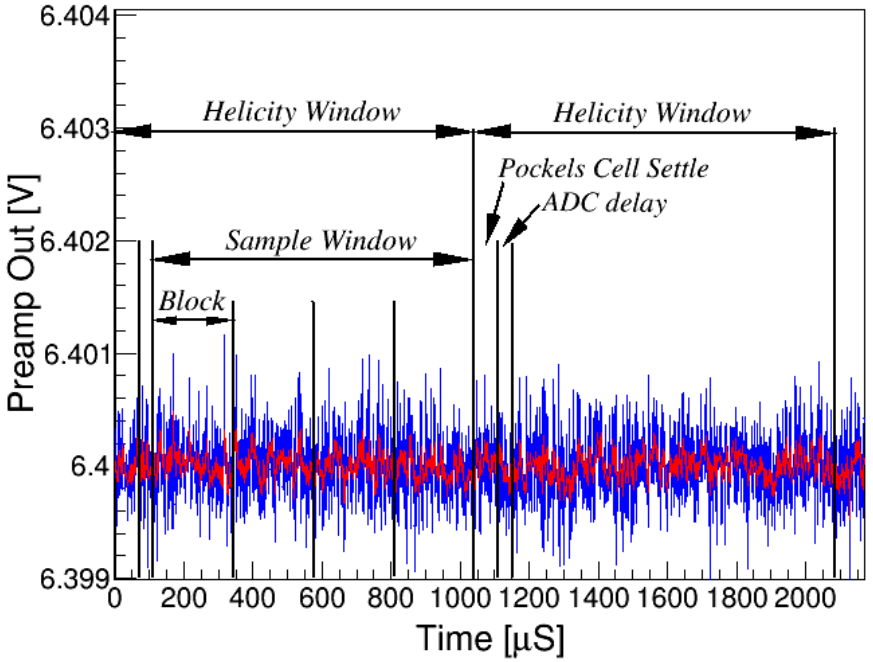
Important open issues:

- Real yield predictions (incl. background) from all detectors (not just Møller ring); SM too.
- PMT choice decision needed soon
- Cable lengths: Where will be put the preamps ? Where will be put the ADCs ?
- Interface with the system: Universal clock; Helicity gate; Data transfer connection/protocol; cables; connectors; etc.
- BCMs: Do we still need to have the same electronics for the BCMs ? If so, in what way, with what requirements?

Basic Acquisition Scheme (for new people)

- Detector yields are integrated (summed) over each helicity state
- Raw asymmetries are formed from differences between positive and negative helicity states within a quartet
- Quartet asymmetries are histogrammed

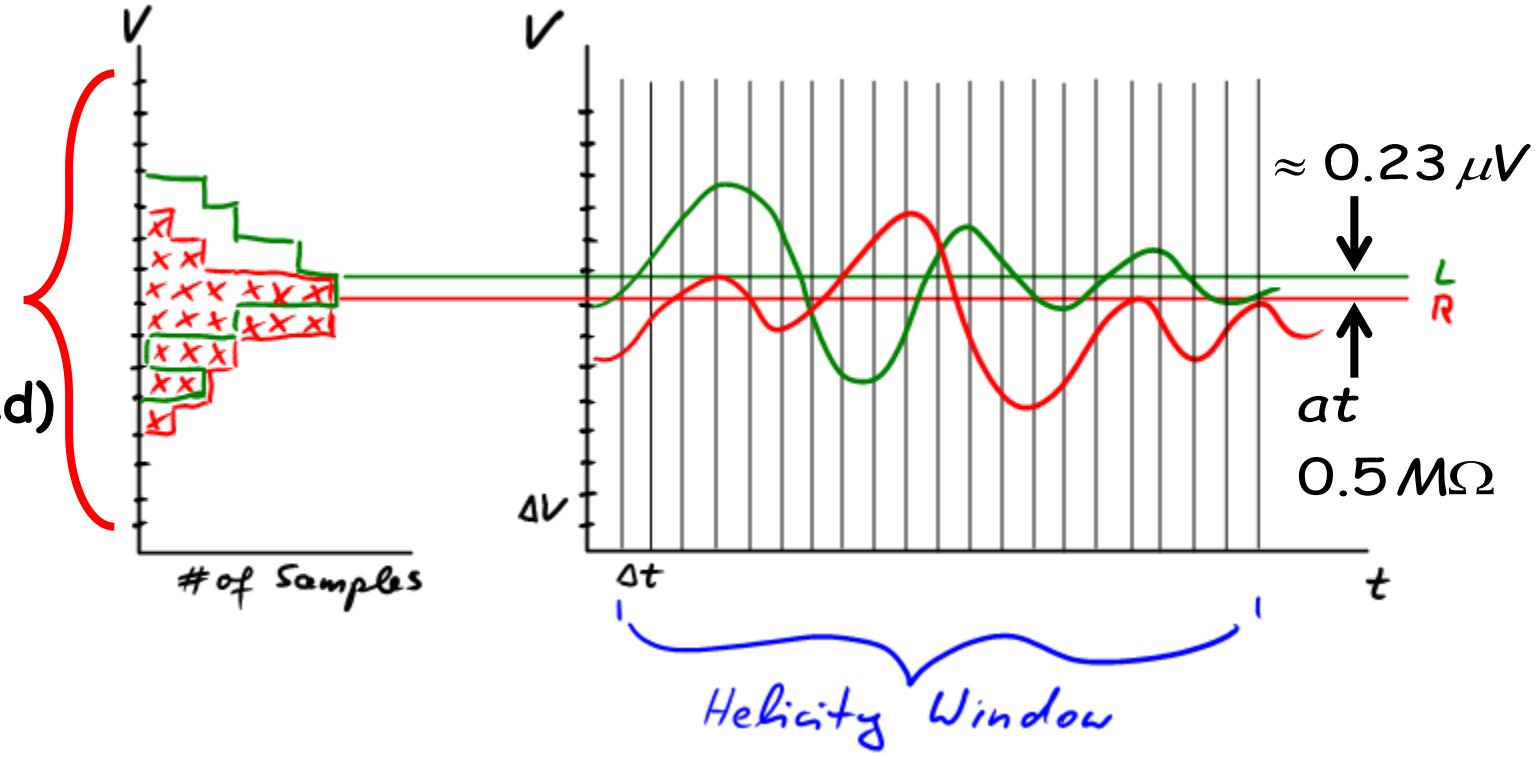




Basic Acquisition Scheme (for new people)

Digitization:

ADC range and resolution (0 suppressed)



18 bit resolution: $\Delta V = \frac{4V}{2^{17}} \approx 30\mu V$